ABSTRACT OF THE DISCLOSURE

A semiconductor memory device has a cell array, first normal elements each defined within the cell array as a group of memory cells arranged in a first direction of the cell array, second normal elements each defined within the cell array as a group of memory cells arranged in a second direction of the cell array, each the second normal element selecting a memory cells in operative association with a corresponding one of the first normal elements, first redundant elements disposed for replacement of defective first normal elements within the cell array, and second redundant elements disposed for replacement of defective second normal elements within the cell array. There are defined within the cell array a first repair regions as a group of first normal elements with permission of replacement by each first redundant element and second repair regions defined within the cell array as a group of second normal elements with permission of replacement by each second redundant element. Whether each of simultaneously activated two first normal elements is replaced by the first redundant element is controlled independently of each other; in addition, at least one of the second normal elements, which repairs a defective second normal element within one of the first repair regions including one of the simultaneously activated at least two first normal elements, does not intersect the one of the simultaneously activated at least two first

normal elements.